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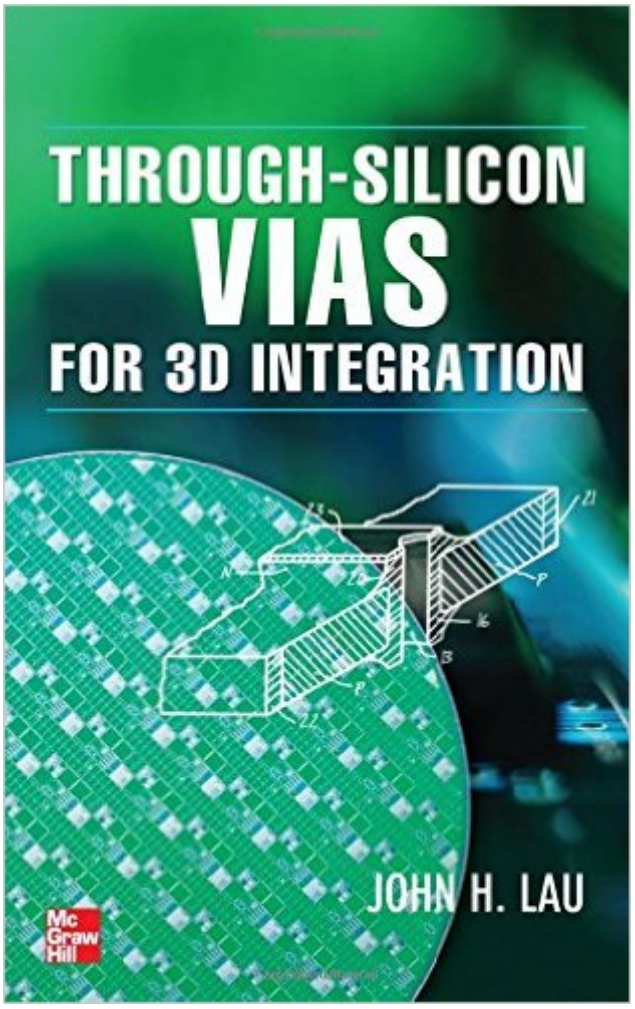

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Synopsis

A comprehensive guide to TSV and other enabling technologies for 3D integration Written by an expert with more than 30 years of experience in the electronics industry, Through-Silicon Vias for 3D Integration provides cutting-edge information on TSV, wafer thinning, thin-wafer handling, microbumping and assembly, and thermal management technologies. Applications to highperformance, high-density, low-power-consumption, wide-bandwidth, and small-form-factor electronic products are discussed. This book offers a timely summary of progress in all aspects of this fascinating field for professionals active in 3D integration research and development, those who wish to master 3D integration problem-solving methods, and anyone in need of a low-power, wide-bandwidth design and high-yield manufacturing process for interconnect systems. Coverage includes: Nanotechnology and 3D integration for the semiconductor industry TSV etching, dielectric-, barrier-, and seed-layer deposition, Cu plating, CMP, and Cu revealing TSVs: mechanical, thermal, and electrical behaviors Thin-wafer strength measurement Wafer thinning and thin-wafer handling Microbumping, assembly, and reliability Microbump electromigration Transient liquid-phase bonding: C2C, C2W, and W2W 2.5D IC integration with interposers 3D IC integration with interposers Thermal management of 3D IC integration 3D IC packaging

Book Information

Hardcover: 512 pages

Publisher: McGraw-Hill Education; 1 edition (October 11, 2012)

Language: English

ISBN-10: 0071785140

ISBN-13: 978-0071785143

Product Dimensions: 6.3 x 0.9 x 9.3 inches

Shipping Weight: 1.8 pounds (View shipping rates and policies)

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